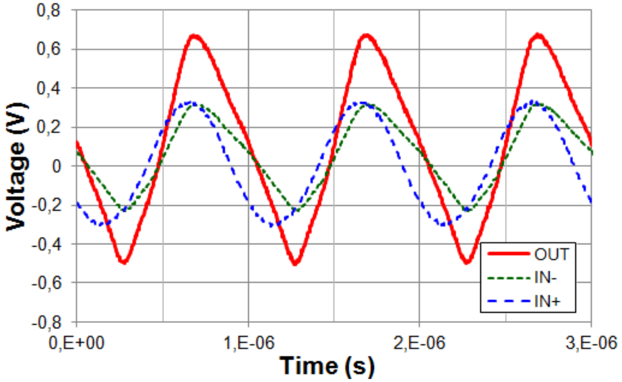
A CASE STUDY TO APPREHEND RF SUSCEPTIBILITY OF OPERATIONAL AMPLIFIERS



A. Boyer[1,2], Etienne Sicard[1]

[1] INSA Toulouse, University of Toulouse, 31077 Toulouse, France
[2]LAAS-CNRS, 7 avenue du colonel Roche, 31077 Toulouse, France
www.ic-emc.org

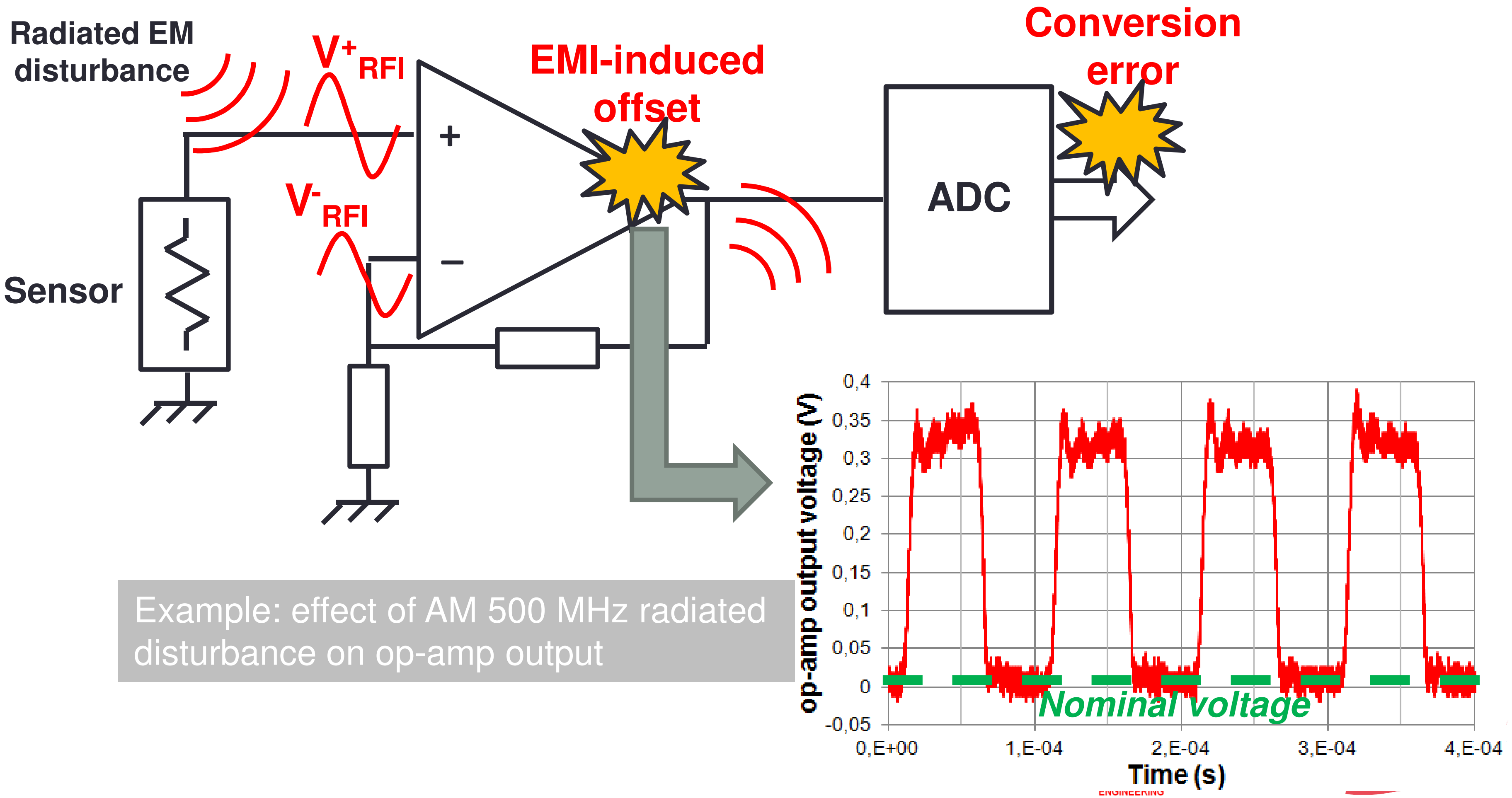
Co-funded by the
Erasmus+ Programme
of the European Union

Outlines

- Purpose
- Experimental results
- Failure analysis
- Modeling op-amp susceptibility
- Validation of the model
- Conclusion

Purpose

- Analog amplifiers very common in signal conditioning
- Very sensitive to out-of-band electromagnetic disturbance, specifically differential inputs



Example: effect of AM 500 MHz radiated disturbance on op-amp output

Purpose

- Many researches on modeling of the failure mechanisms and op-amp design improvement
- Issue still misunderstood by most electronic designers
- No simple models available to validate their design

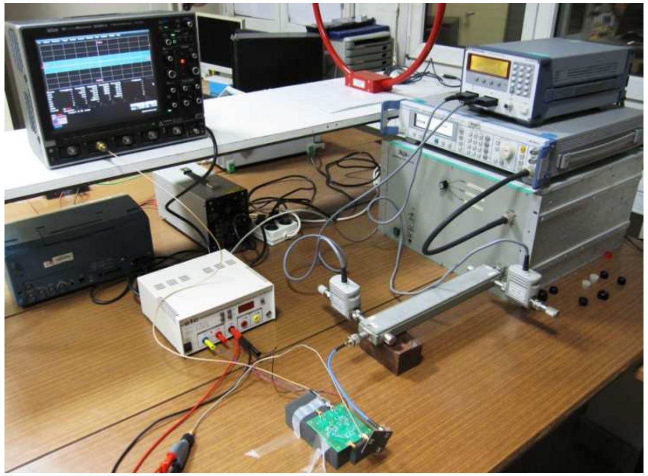
✓ Dedicated training to clarify this problem (observation by measurement, modeling, evaluation of design guidelines)

✓ Based on low-cost demo board and SPICE simulation

- J. G. Tront, J. J. Whalen, C. E. Larson, J. M. Roe, "Computer-Aided Analysis of RFI Effects in Operational Amplifiers", IEEE Trans. on EMC, 21, (4), Nov. 1979
- D. Golzio, S. Graffi, G. Masetti, "New Circuit Modeling of Operational Amplifiers", IEEE Int. Symp on EMC, USA, 1989
- F. Fiori, "A New Nonlinear Model of EMI-Induced Distortion Phenomena in Feedback CMOS Operational Amplifiers", IEEE Trans on EMC, 44, (4), Nov. 2002
- J. M. Redouté, M. Steyaert, EMC of Analog Integrated Circuits, Springer, 2010
- …

Purpose

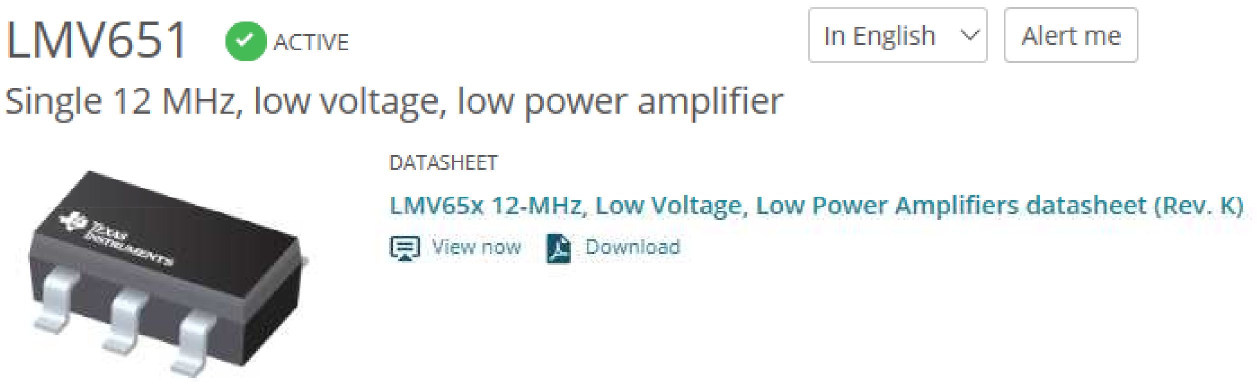
- Contents of the training:
  - ✓ Illustration on a real case-study
  - ✓ Presentation of conducted immunity test-bench
  - ✓ Analysis of the failure mechanisms
  - ✓ EMI-hardened vs. non-hardened op-amp
  - ✓ Building of susceptibility models of op-amp
  - ✓ Simulation of DPI tests on op-amp
  - ✓ Evaluation of design guidelines for improved immunity



www.ic-emc.org

Presentation of the experiments

- Two comparable amplifiers from www.ti.com

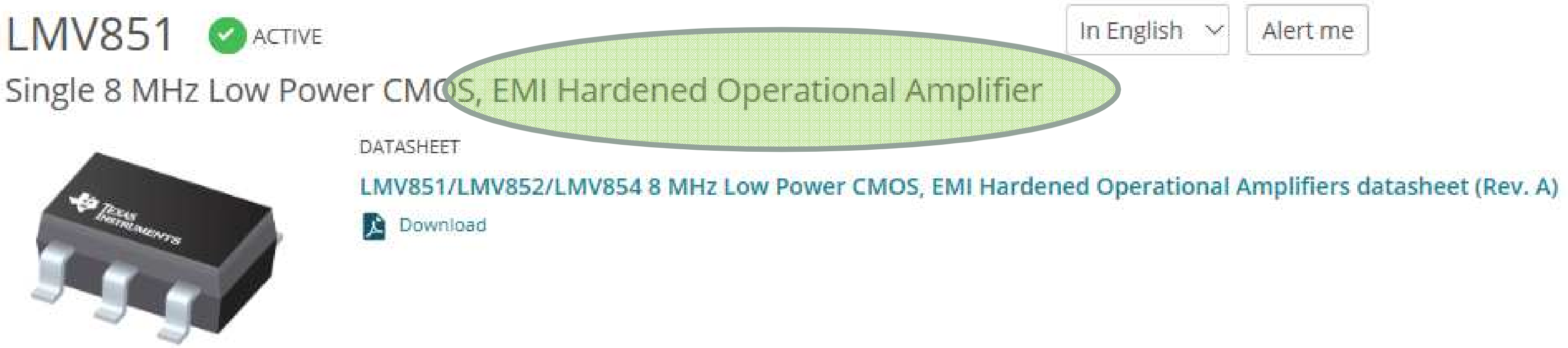


LMV651

Single 12 MHz, low voltage, low power amplifier

DATASHEET

LMV65x 12-MHz, Low Voltage, Low Power Amplifiers datasheet (Rev. K)



LMV851

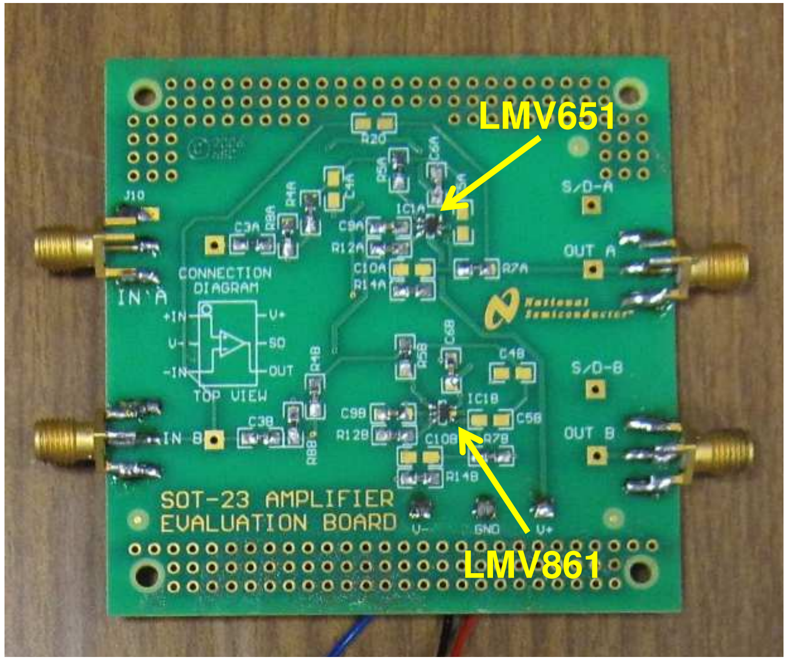
Single 8 MHz Low Power CMOS, EMI Hardened Operational Amplifier

DATASHEET

LMV851/LMV852/LMV854 8 MHz Low Power CMOS, EMI Hardened Operational Amplifiers datasheet (Rev. A)

Presentation of the experiments

- TI’s universal op amp evaluation board 551012875
- Comparison of conducted immunity on V+ and Vout



EMI Hardened

Characteristics	LMV651	LMV861
Power supply	+/- 2.5 V	+/- 2.5 V
Static gain	93 dB	110 dB
GBW product	12 MHz	30 MHz
Slew rate +/- (not specified by datasheet)	3.6 / -2.2 V/µs	21.2 / -24.2 V/µs
Max. input offset voltage	1.5 mV	1 mV
CMRR	100 dB	93 dB
PSRR	95 dB	93 dB
EMIRR	Not defined	70 - 110 dB (400-2400 MHz)

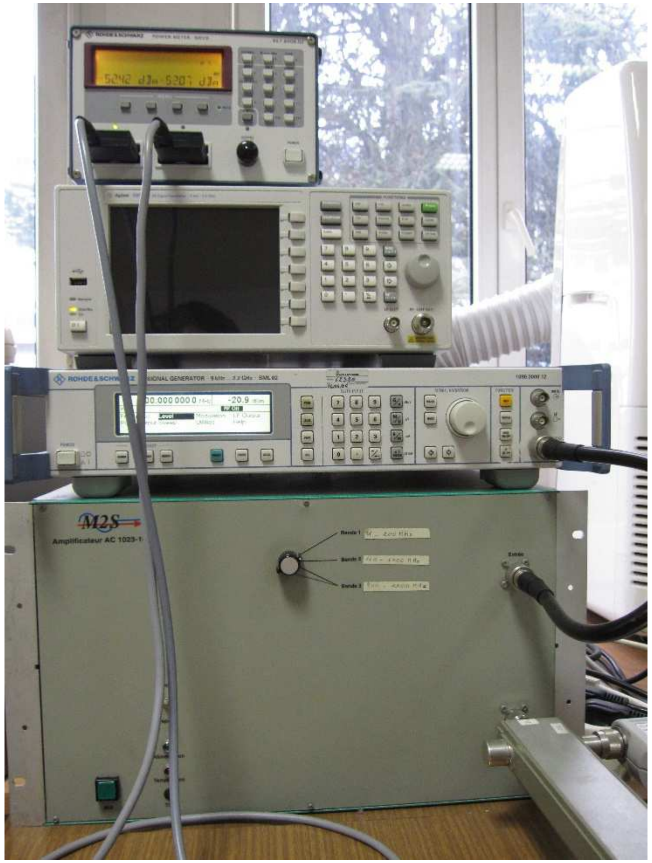
$$EMIRR = \frac{\Delta V_{pp}}{V_{offset\_out}}$$

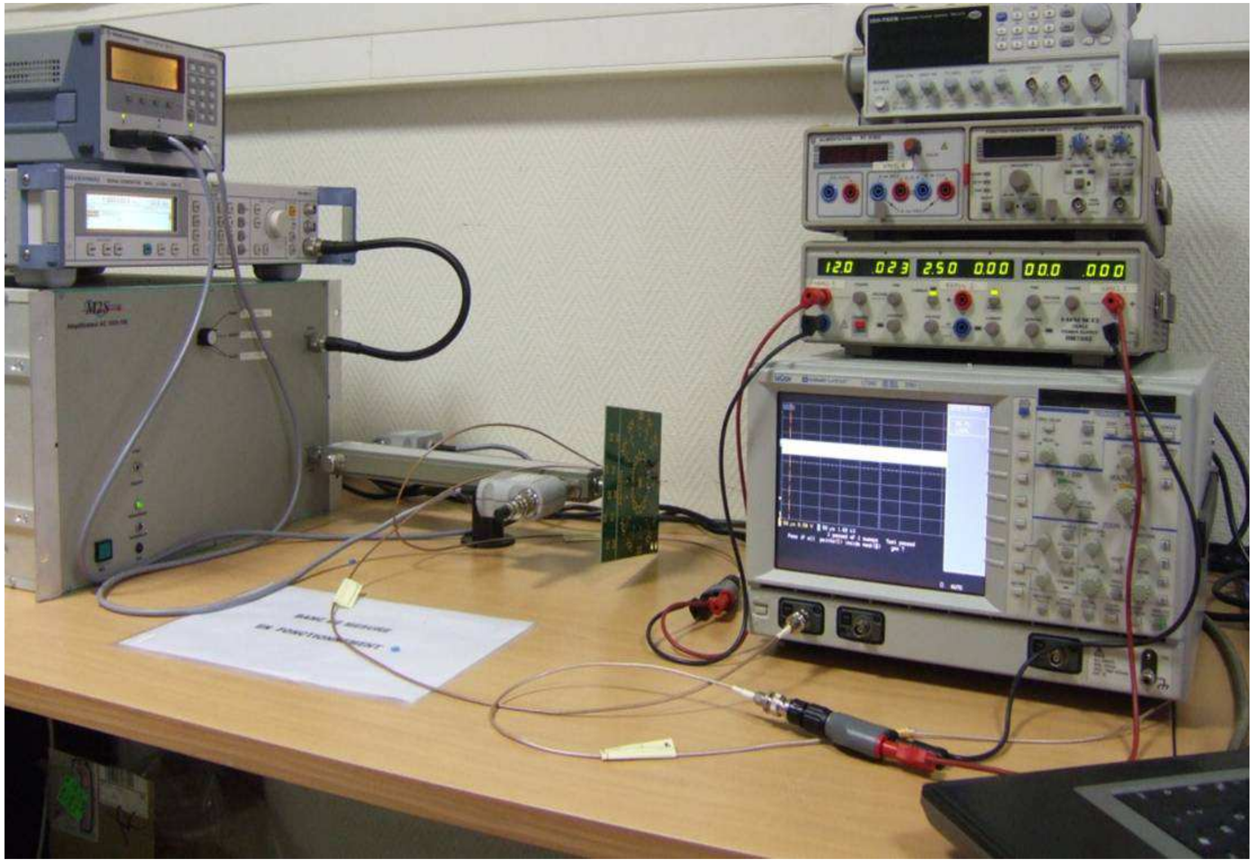
Applied disturbance amplitude

Induced output offset

Presentation of the experiments

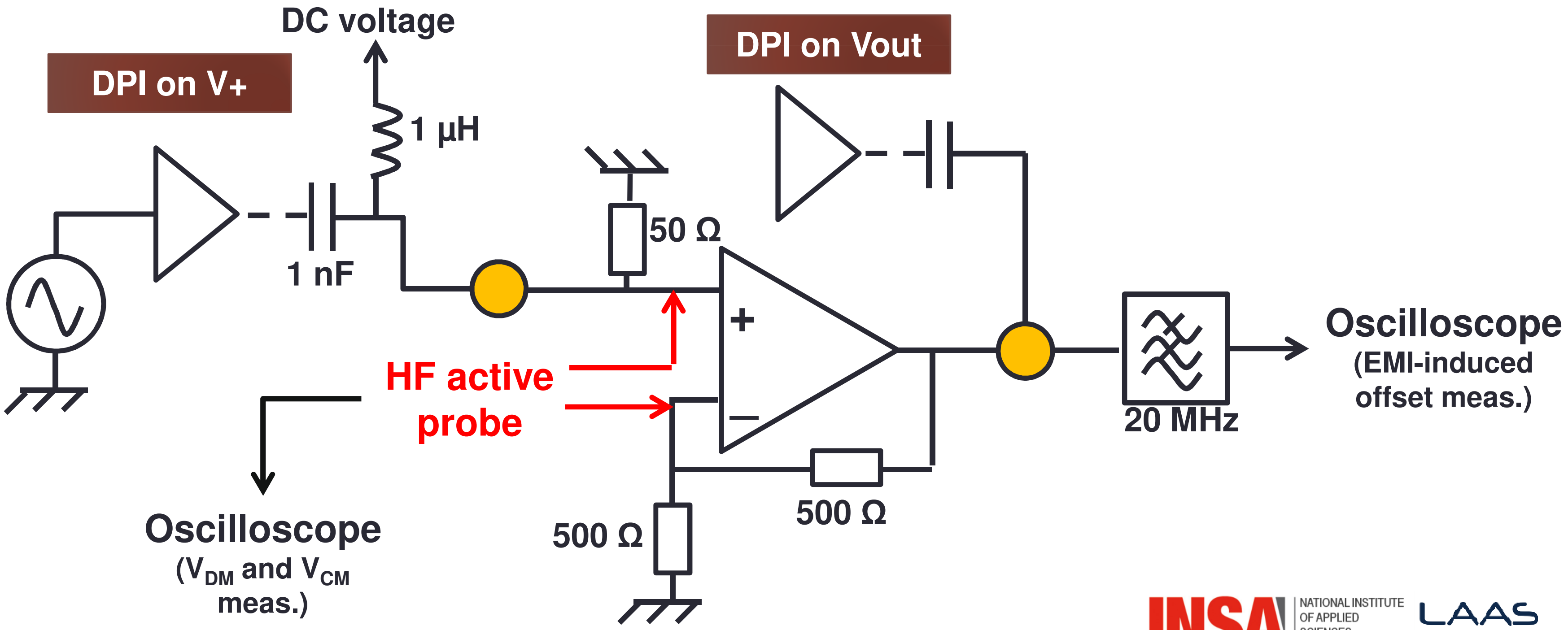
- DPI test bench at INSA
- Very close to IEC 62132-4 Direct Power Injection tests from 1 MHz to 1 GHz
- Forward power = 25 dBm (0,3W)





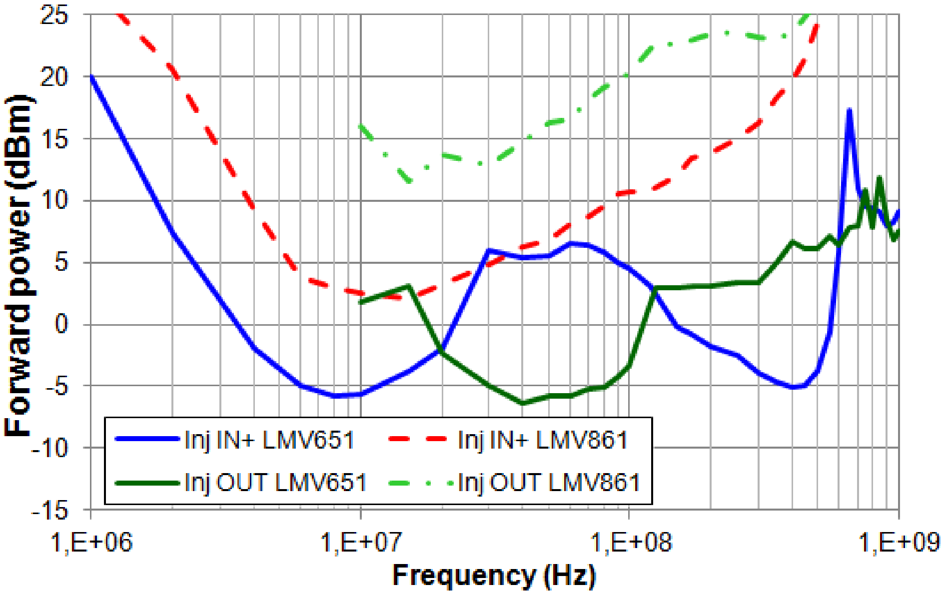
Experimental results

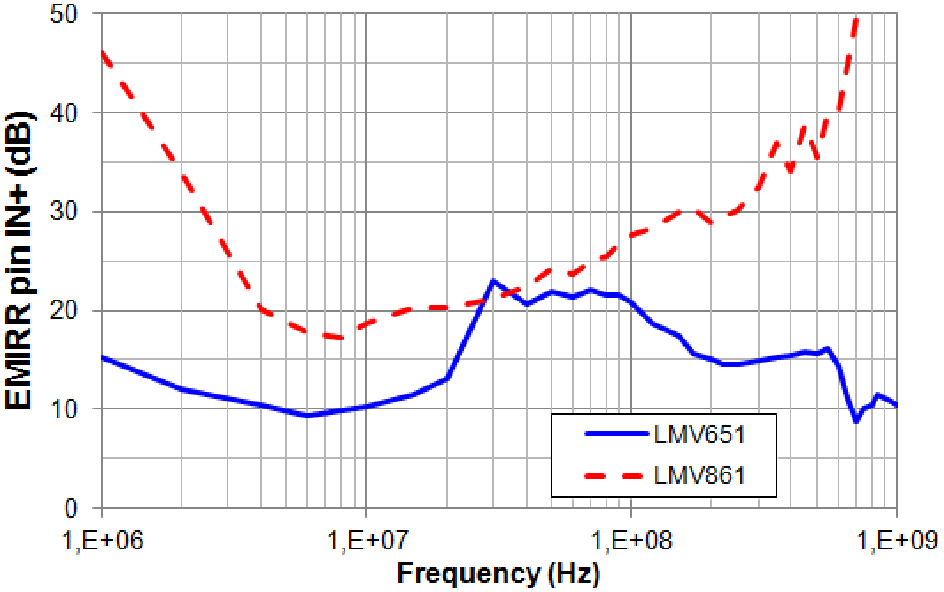
- Op-amp mounted on non-inverting amplifier configuration (gain x2)
- Injection on non-inverting input V+ and Vout.
- Failure criterion: +/-100 mV output offset



Experimental results

- Susceptibility level and EMIRR measurements on IN+ and Vout
- EMI-hardened version is the most robust, except between 25 and 60 MHz.
- Different types of failures appear depending on frequency





INSA NATIONAL INSTITUTE OF APPLIED SCIENCES TOULOUSE
DEPARTMENT OF COMPUTER & ELECTRICAL ENGINEERING

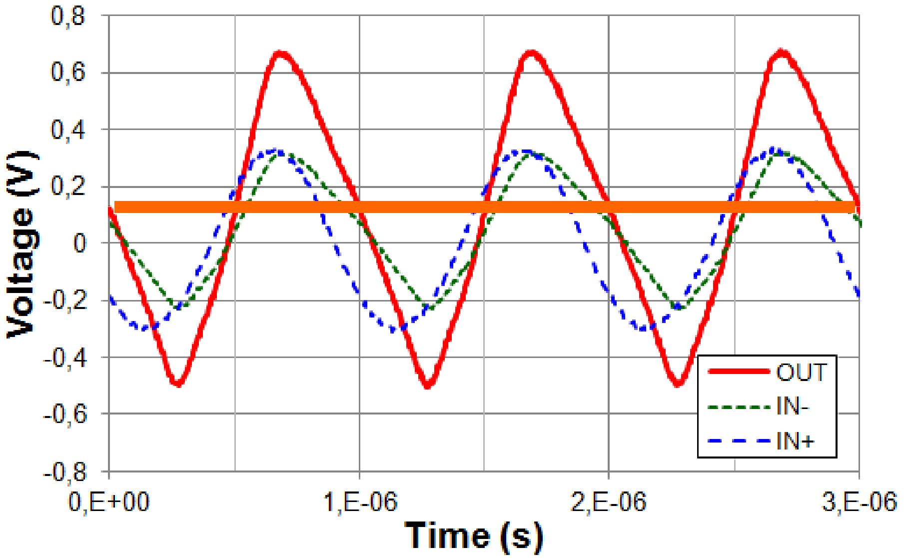
LAAS CNRS

Failure analysis

- Low-frequency DPI failure: slew-rate asymmetry

LMV651

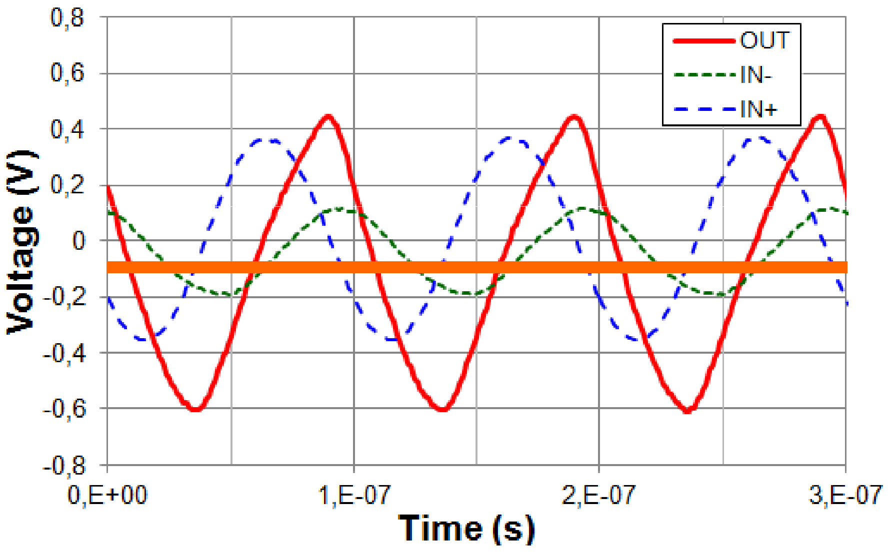
SR+ > SR- (3.6 / -2.2 V/µs)



Positive offset

LMV861

SR+ < SR- (21.2 / -24.2 V/µs)



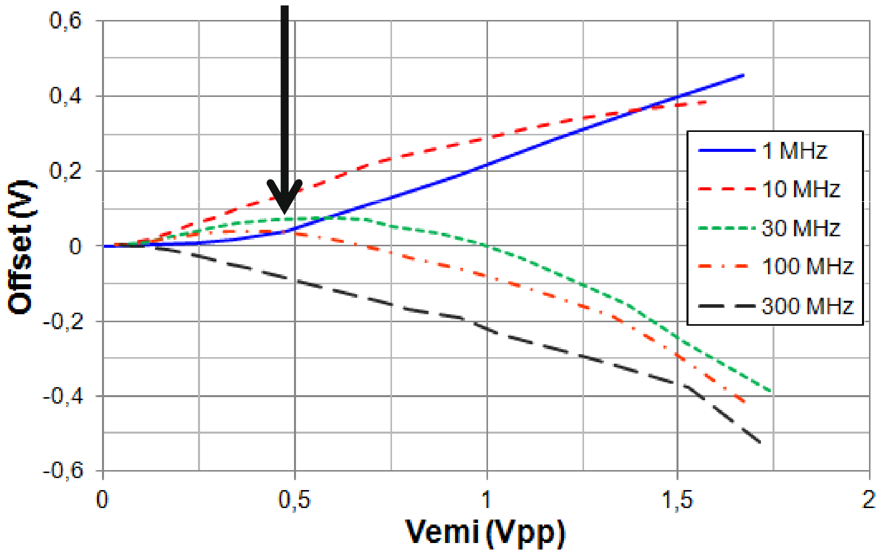
Negative offset

Failure analysis

- For both op-amps, three failure mechanisms are observed:

1. Up to some tens of MHz : positive offset, quasi-linear increase with EM disturbance amplitude (**slew rate asymmetry**)
2. Above some tens of MHz : negative offset, rapid increase with EM disturbance amplitude (**weak distortion**)
3. High frequency and large disturbance level : saturation of the output (**asymmetrical cut-off**)

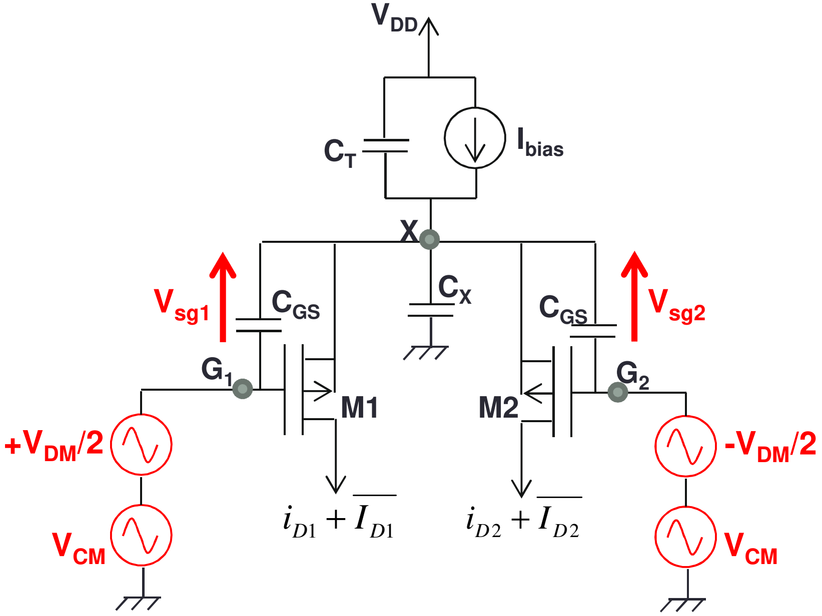
Compensation of failure mode 1 by failure mode 2



Evolution of EMI-induced offset vs. disturbance amplitude and frequency

Failure analysis

- High-frequency DPI failure: weak distortion brought by input differential pair



- ✓ Non linear behavior of MOS transistor leads to rectification of induced RF current
- ✓ Generation of drain current offsets (I_{D1} and I_{D2})
- ✓ Induced drain current imbalance ΔI_D:

$$\Delta I_D = \overline{I_{D1}} - \overline{I_{D2}} = \frac{\mu_P C_{ox}}{2}\frac{W}{L}\left(\overline{v_{sg1}^2} - \overline{v_{sg2}^2}\right)$$

- ✓ Drain current imbalance if:
  - Diff. mode voltage $V_{DM} \neq 0$
  - Common-mode voltage $V_{CM} \neq 0$

- ✓ Theoretical EMI-induced input-related voltage offset:

$$V_{off\_in} = \frac{-1}{2\left|V_{sg} - V_T\right|}\left|V_{DM}V_{CM}H_{CM}\right|\cos\left(\phi + \arg\left(H_{CM}\right)\right)$$

With: $H_{CM} = \frac{V_{sg}}{V_{CM}} = \frac{j\omega\left(C_T + C_X\right)}{j\omega\left(2C_{gs} + C_T + C_X\right) + 2g}$ and Φ is the phase between V_{DM} and V_{CM}

High-pass behavior

Modeling op-amp susceptibility

- No susceptibility models provided by manufacturers (even the slew rate asymmetry is not given)
- Failure mechanisms are based on complex mechanisms, whose accurate modeling requires unknown information for end-users

→ Propose a simplified equivalent electrical SPICE-based model built from measurement results (no extra measurement and rapid modeling process)

→ Susceptibility simulation made with IC-EMC freeware

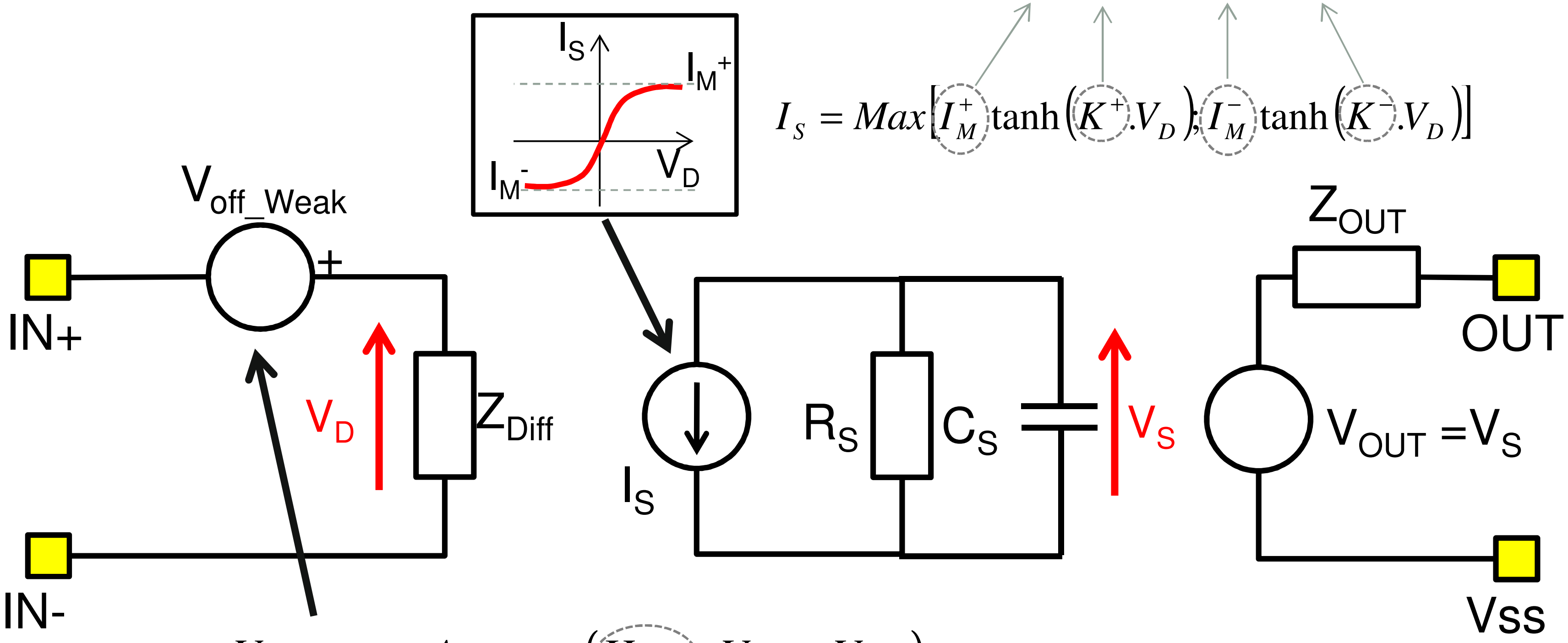
Modeling op-amp susceptibility

- Proposed equivalent model for slew rate asymmetry and weak distortion effects:

1. Slew rate asymmetry

Calculated from measurements

$$I_S = Max\left[I_M^+ \tanh\left(K^+ . V_D\right); I_M^- \tanh\left(K^- . V_D\right)\right]$$



$$V_{off\_weak} = Average\left(H_{CM} \times V_{DM} \times V_{CM}\right)$$

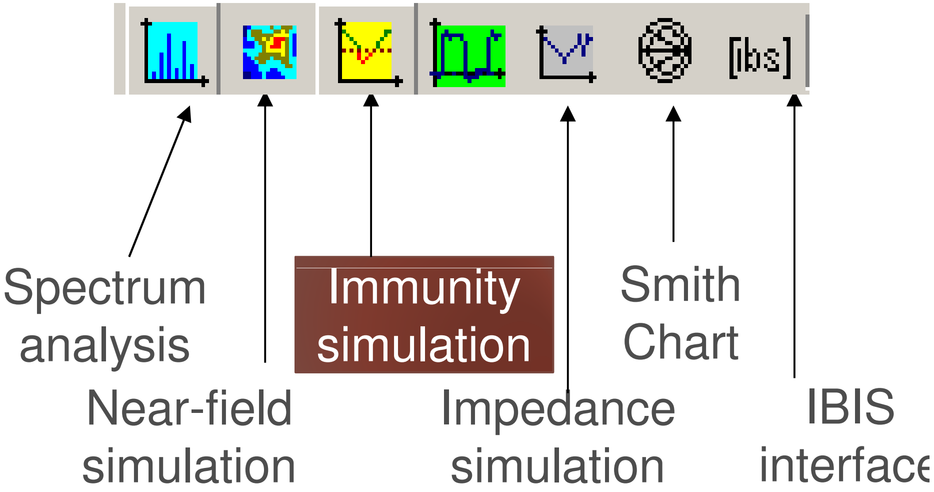
2. Weak distortion

Equivalent filter fitted from measurements

Modeling op-amp susceptibility

- IC-EMC, a tool for simulating emission & susceptibility of integrated circuits
  - A schematic editor
  - An interface to WinSpice
  - A post-processor to compare simulated with measured spectrum
  - Freeware, online www.ic-emc.org
  - 250 pp documentation, 15 case studies

Key tools



Spectrum analysis

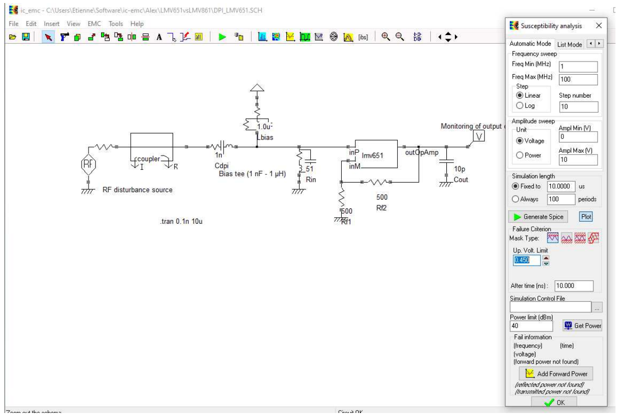
Near-field simulation

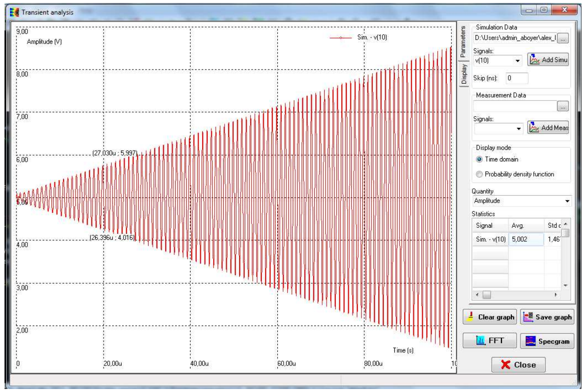
Immunity simulation

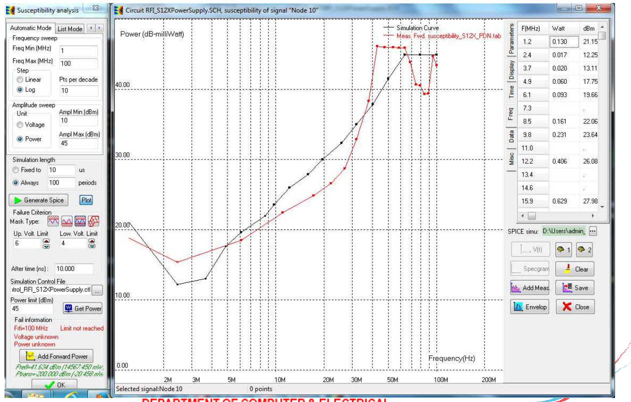
Impedance simulation

Smith Chart

IBIS interface

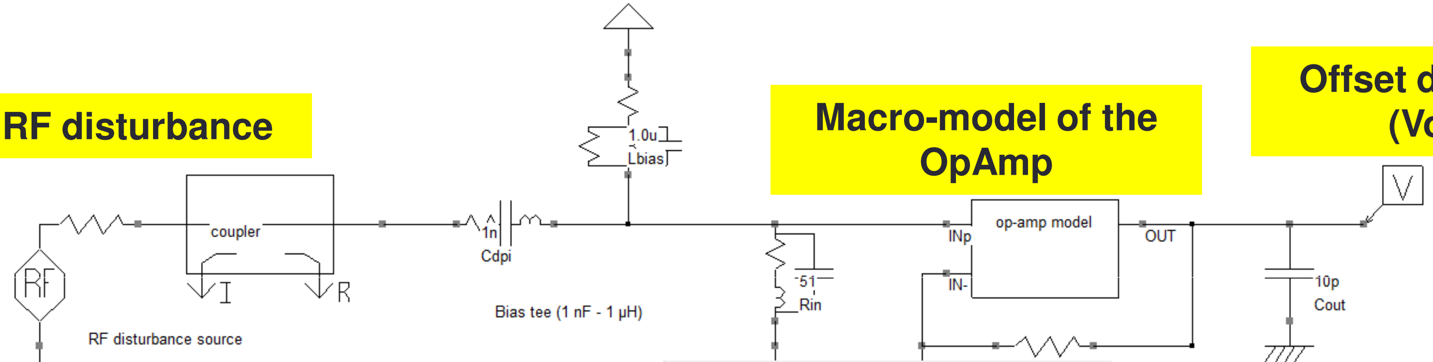






Modeling op-amp susceptibility

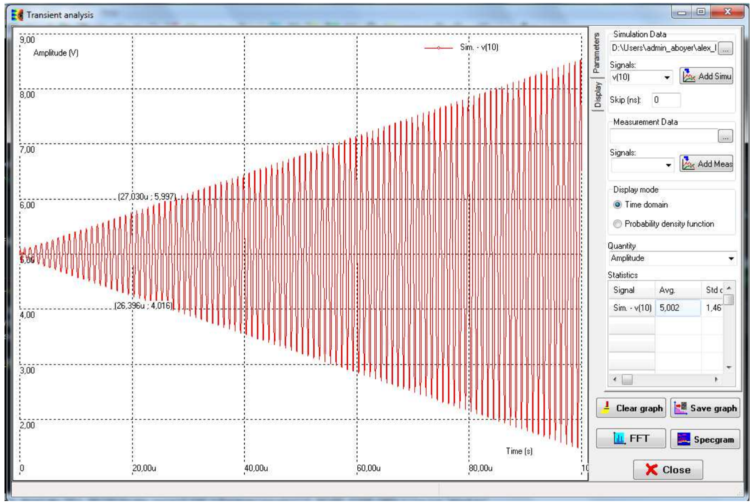
- Op-Amp macro model described using SPICE "E" elements (any formula)
- DPI simulation in IC-EMC using RF disturbance & coupler
- Iterative simulations with varying frequencies (10 per decade)



RF disturbance

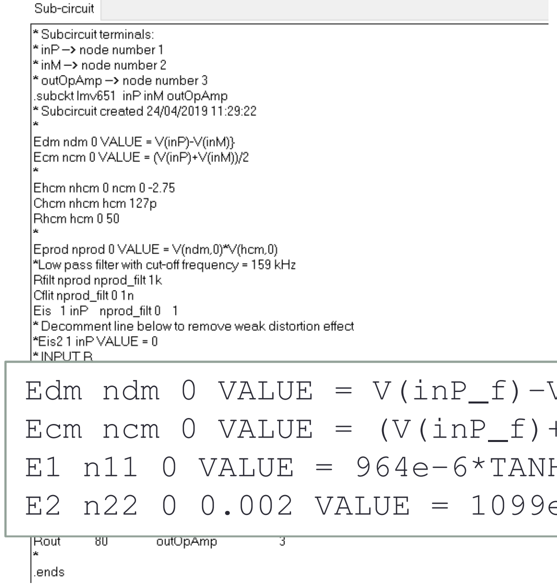
Macro-model of the OpAmp

Offset detection (Vout)



Simulation Data: D:\Users\admin_aboyer\alex_l
Signals: v(10)
Skip (ns): 0
Measurement Data
Signals:
Display mode: ● Time domain ○ Probability density function
Quantity: Amplitude
Statistics

Signal	Avg.	Std c
Sim. - v(10)	5,002	1,46



```
* Subcircuit terminals:
* inP --> node number 1
* inM --> node number 2
* outOpAmp --> node number 3
.subckt lmv651  inP inM outOpAmp
* Subcircuit created 24/04/2019 11:29:22
*
Edm ndm 0 VALUE = V(inP)-V(inM)}
Ecm ncm 0 VALUE = (V(inP)+V(inM))/2
*
Ehcm nhcm 0 ncm 0 -2.75
Chcm nhcm hcm 127p
Rhcm hcm 0 50
*
Eprod nprod 0 VALUE = V(ndm,0)*V(hcm,0)
*Low pass filter with cut-off frequency = 159 kHz
Rfilt nprod nprod_filt 1k
Cflit nprod_filt 0 1n
Eis   1 inP    nprod_filt 0    1
* Decomment line below to remove weak distortion effect
*Eis2 1 inP VALUE = 0
* INPUT R
```

```
Edm ndm 0 VALUE = V(inP_f)-V(inM_f)}
Ecm ncm 0 VALUE = (V(inP_f)+V(inM_f))/2
E1 n11 0 VALUE = 964e-6*TANH(9.18*V(1,inM_f))
E2 n22 0 0.002 VALUE = 1099e-6*TANH(8.06*V(1,inM_f))
```

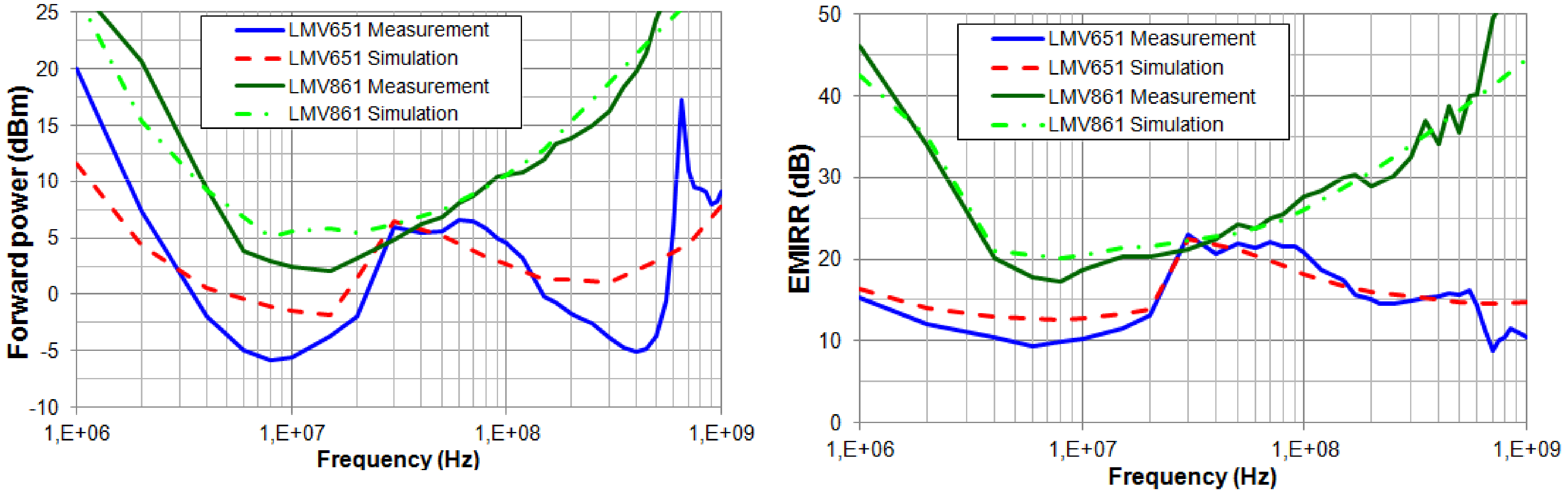
```
Rout        80          outOpAmp            3
*
.ends
```

INSA OF APPLIED SCIENCES TOULOUSE
DEPARTMENT OF COMPUTER & ELECTRICAL ENGINEERING

LAAS CNRS

Validation of the models

- Comparison between measurements and simulations of LMV651 and LMV861 DPI level and EMIRR (non-inverter configuration).
- Injection on non-inverting input

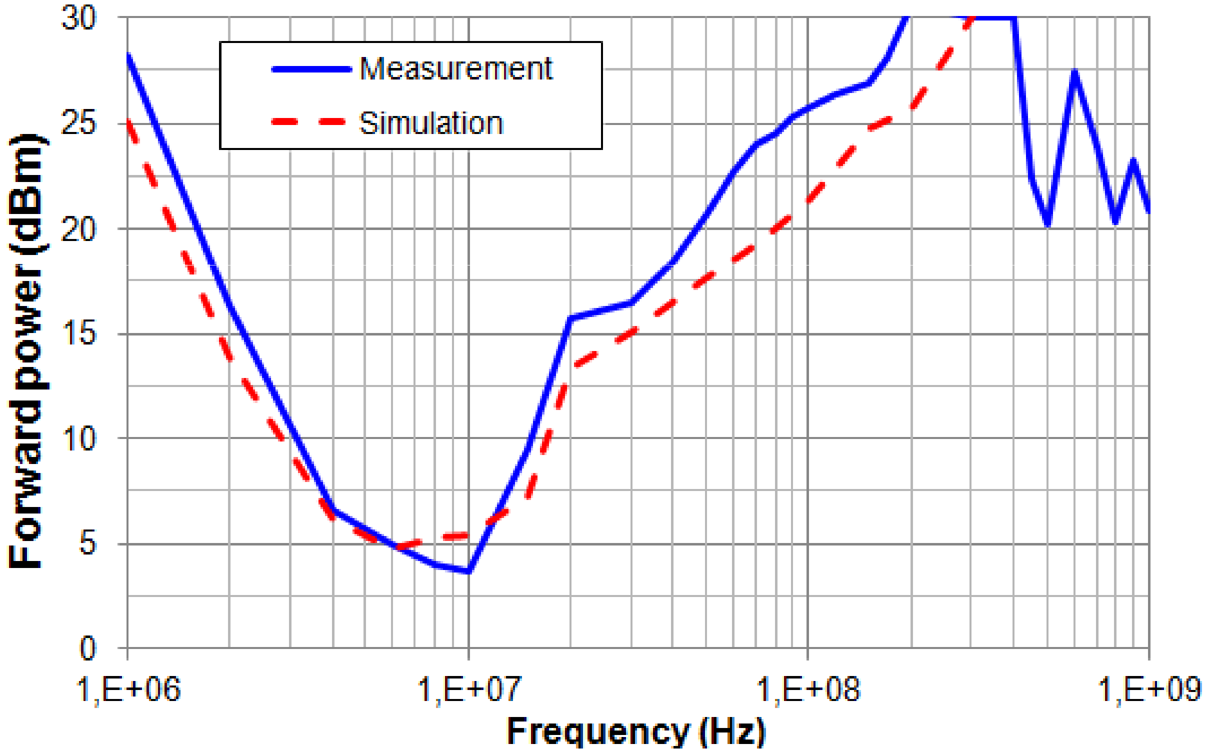


- Quite good agreement between 10 and 500 MHz.
- Loss of accuracy around 10 MHz: limitation of slew rate model
- Loss of accuracy above 500 MHz: lack of models of coupling between pins

INSA NATIONAL INSTITUTE OF APPLIED SCIENCES TOULOUSE
DEPARTMENT OF COMPUTER & ELECTRICAL ENGINEERING
LAAS CNRS

Validation of the models

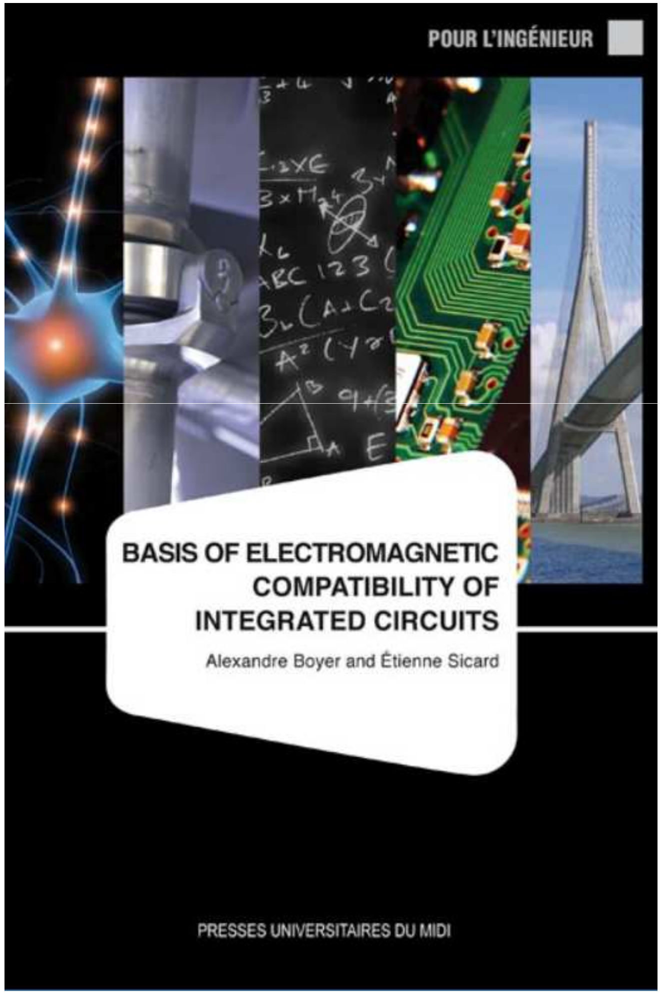
- DPI test in another configuration: voltage follower and additional external low-pass filter on non-inverting input pin (LMV651)



- Good agreement up to 400 MHz
- Above 400 MHz: limitation of the model

Training scenario & feedback

- 2-hours measurement :
  - Discovery of injection test bench
  - Single-frequency DPI injection to highlight failure modes
  - Comparison between standard & EMI-hardened OpAmps
- 2-hours simulation;
  - Simulation of DPI test bench on a resistive load
  - Simulation of DPI test bench on a OpAmp model
- Positive feedback from attendees (90% satisfied/100 students)



POUR L'INGÉNIEUR

BASIS OF ELECTROMAGNETIC COMPATIBILITY OF INTEGRATED CIRCUITS

Alexandre Boyer and Étienne Sicard

PRESSES UNIVERSITAIRES DU MIDI

Conclusion

- A practical training dedicated to the susceptibility of op-amps to electromagnetic disturbances:
  - Illustration of typical failure mechanisms
  - Building a simple equivalent electrical model
  - Test different EMI reduction techniques (EMI-robust op-amp, filtering)
- The simple op-amp equivalent model provides acceptable prediction results for op-amp end-users to anticipate EMI issues up to 500 MHz.

THANK YOU FOR YOUR ATTENTION

alexandre.boyer@insa-toulouse.fr

www.ic-emc.org